Q.P. Code: 16CS510 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY: PUTTUR

(AUTONOMOUS)

B.Tech II Year II Semester Supplementary Examinations July-2021

COMPUTER ORGANIZATION

(Common to CSE & CSIT)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Explain about Instruction Cycle with neat diagram.	**6M**
	b	Write in detail about the Basic Operational Concepts with neat diagram.	**6M**

OR

2	**a**	Explain detail about Instruction Cycle with neat sketch.	**6M**
	b	Write about Memory-Reference-Instruction.	**6M**

UNIT-II

3		Draw the H/W Flowchart and H/W Algorithm for Multiplication for positive numbers with a suitable example.	**12M**

OR

4		Draw the H/W Flowchart and H/W Algorithm for Multiplication for signed numbers (Booth Multiplication) with a suitable example.	**12M**

UNIT-III

5	**a**	Show that the block diagram of the hardware that implements the following register transfer statement P: R2←R1.	**6M**
	b	Explain about the way of constructing a 4 line common bus system using multiplexers with a neat diagram.	**6M**

OR

6		Explain in details about all 3 types of Shift Register Operations.	**12M**

UNIT-IV

7	**a**	Explain about Memory Hierarchy.	**6M**
	b	Explain about Memory Management Requirements.	**6M**

OR

8		Explain in detail about Cache Memory with Page Replacement Algorithms.	**12M**

UNIT-V

9		Explain about Inter Processor Arbitration with neat sketch.	**12M**

OR

10		Explain about Inter Process Communication & Synchronization in detail.	**12M**

*** END ***